PHASE-LOCKED CRYSTAL OSCILLATORS

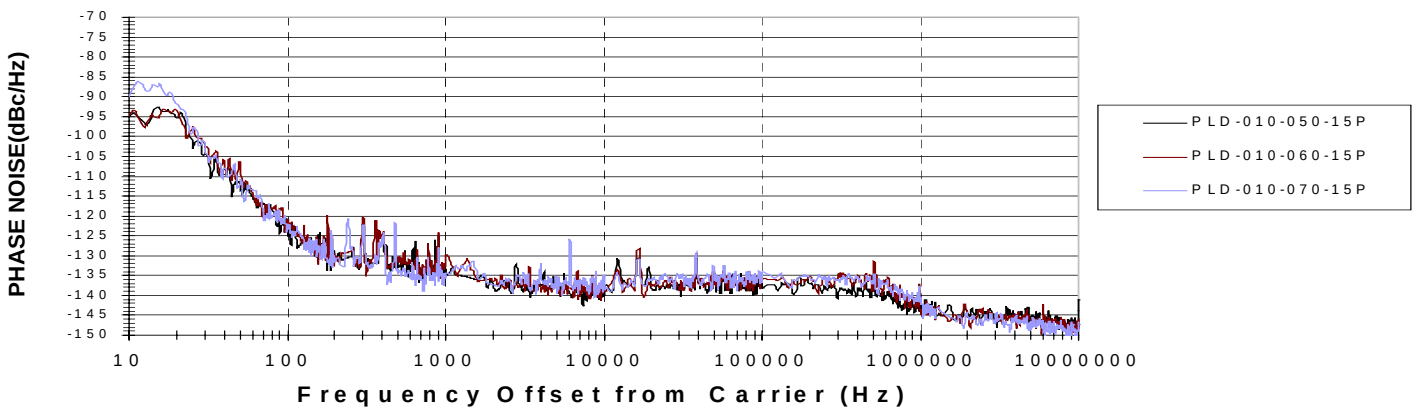
PLD SERIES:
30 – 165 MHz (PLD)

FEATURES

- Low phase noise design
- Fractional frequency division available
- +13 dBm standard output power

OPTIONS

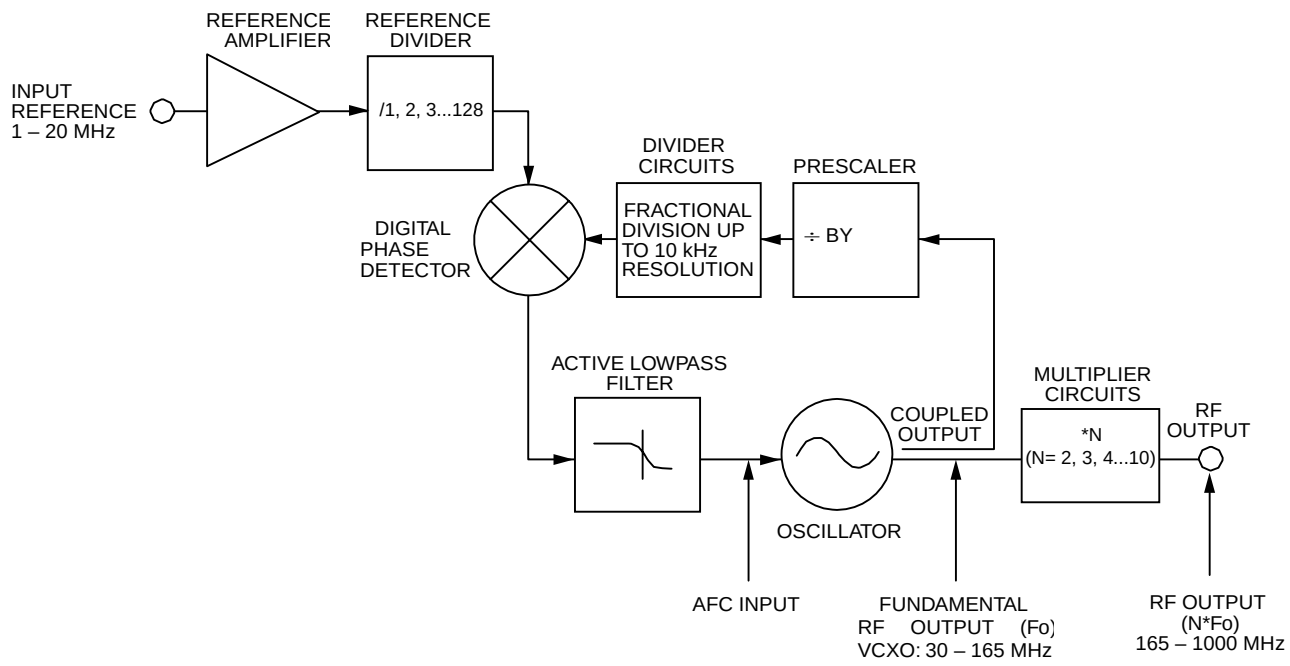
- Higher output power
- TTL output
- Coupled RF output



ELECTRICAL SPECIFICATIONS

Output frequency range Fundamental (PLD)	30 – 130 MHz
Output power	+13 dBm minimum
Output power variation	±1 dB maximum
Phase noise	See graph
Harmonic output	-20 dBc maximum
Spurious output	-70 dBc maximum
Input reference frequency	1 – 20 MHz
Input power level	0 ±3 dBm
Input impedance	50 ohms
Load VSWR	1.5:1 nominal
DC power requirements (Note 1)	+15, or +20volts @ 250 mA +5 volts @ 200 mA

BLOCK DIAGRAM



ORDERING INFORMATION

Output frequency 30 – 165 MHz

PLD - ___ ___ ___ - ☐☐☐☐ - ___ - ___ **P**

Input freq. (MHz)	Output freq. (MHz)	Alarm Option	Supply Voltage

ALARM OPTIONS

0. 0 Volts In Lock, +V out of Lock
3. TTL; Low in Lock, High out of Lock
4. TTL; High in Lock, Low out of Lock

SUPPLY VOLTAGE OPTIONS

15. +15 VDC.
20. +20 VDC.

MECHANICAL SPECIFICATIONS

Weight
- Fundamental..... 250 grams nominal
- Multiplied ..... 300 grams nominal

RF connectors ..... SMA female
DC connectors..... Feedthru filter

ENVIRONMENTAL SPECIFICATIONS

Temperature
- Operating ..... 0 to 60°C
- Storage ..... -45 to +85°C

Humidity..... 95% at 40°C noncondensing
Shock (survival) ..... 30 g's, 10 ms pulse
Vibration (survival) ..... 20 to 2000 Hz random to 4 g's

OUTLINE DRAWINGS

PLD SERIES (FUNDAMENTAL)